High-Temperature Integrated Circuits with SiC CMOS

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Introduction:
Silicon Carbide (SiC) is a has wide-bandgap semiconductor with very low intrinsic carrier concentration and the ability to grow a native oxide, making it the natural candidate to follow silicon's microelectronics revolution development path, and extend its reach beyond the operational temperature limits of approximately 250 ºC. SiC process technology being relatively new, especially for CMOS, raises material and process-related challenges. We develop high-temperature (HT) devices and circuits with a holistic approach ranging from physics-based device/material/process simulations, to design and layout and fabrication to testing. Our overall goal is become a go-to source for SiC CMOS circuits for long-term reliable HT operation. We also target high performance and smaller feature sizes, with the ultimate goal of creating general purpose circuits (e.g. simple microprocessors) operating at >400 ºC and of much greater complexity than is feasible with JFET or bipolar technology.

Expanding the microelectronic revolution to the HT regime opens up exciting application areas. Data conversion and processing capabilities at HT would enable more robust, easier-to-implement smart sensor systems as system-level architectures, *e.g.* for in-engine monitoring/control systems in jet and rocket engines, and in exhaust systems of traditional car engines. For these as well as in EVs, HT components simplify the overall design by requiring less cooling and signal transfer. The energy industry, particularly in geothermal and nuclear, would benefit from HT sensors and data processing available, as would industrial process monitoring applications and hypersonic aircraft technology.

Process, Device and Circuit Development:
The key to fabricating SiC CMOS integrated circuits is to develop a robust fabrication process. CoolCAD has developed and patented a fabrication process for high temperature SiC based electronics [1,2]. The CMOS circuits are fabricated on a standard N+ wafer, which is topped by an epitaxial structure. We obtain both polarity devices by using an implanted well structure for one of the polarities. The fabrication is performed in-house using a university fab that we have upgraded with a high-temperature furnace and new gas lines for SiC processing. We optimize device and material characteristics using NMOS, PMOS, CMOS, N- and P-MOSCAP devices. Among the circuits we have prototyped for room and high temperatures operation are amplifiers, digital gates, latches and counters, comparators, and analog-to-digital converters. We focus on the following aspects: a) Improve the quality of and thermally harden the *gate dielectric*; b) Identify and implement a *gate stack*, and *doping profiles*, for optimal device characteristics; c) Set processing and materials for *integrating NMOS and PMOS devices on a single substrate*; d) Ensure *electrical symmetry between the NMOS and PMOS devices*; e) Long-term testing for *reliability*.

Fig. 1 shows the IV curves for one of our SiC NMOS devices measured before and after 125 hours of thermal stress at 400 ºC without bias. There is no detectable degradation in device characteristics. Fig. 1 also shows IV curves for an NMOS taken at 300 and 500 ºC, for two PMOS devices at room temperature, and CV curves of three n-MOSCAPs with different material systems. Fig. 1 further shows the operation of a NAND gate and an inverter at 300 ºC and of a CMOS divide-by-2 counter at 500 ºC. Fig. 2 shows the

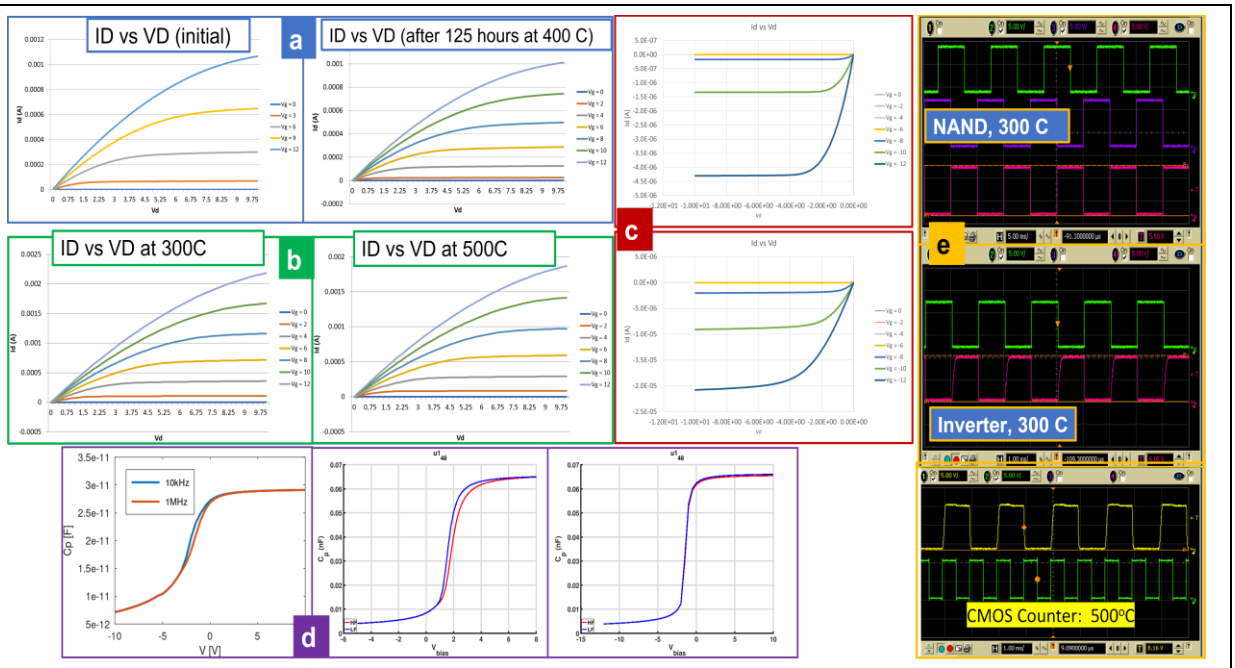

Fig. 1 a) ID-VD curves of SiC NMOS devices at room temperature before/after 125 hours of at 400 ºC. b) ID-VD curves of SiC NMOS devices at 300 and 500 ºC. c) ID-VD curves of SiC PMOS devices. D) CV curves of n-MOSCAPs with SiO_2/Al_2O_3 stack and aluminum gate (left), SiO_2 grown in O_2 and nickel gate (middle), SiO_2 grown in O_2 and annealed in NO, and n-poly gate (right). e) The operation of CMOS NAND and inverter circuits at 300 ºC and of a divide-by-2 counter at 500 ºC.

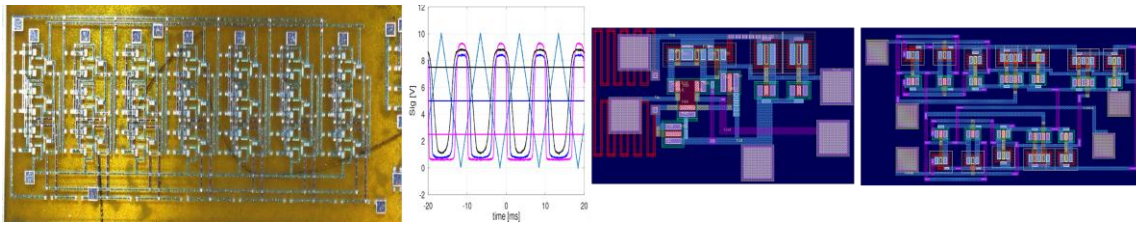

Fig. 2 Left to Right: The microphotograph of a SiC ADC and its operation at 500 ºC; layouts of a comparator and a full adder.

microphotograph of an analog-to-digital converter and its operation at 500 ºC, as well as layouts of a CMOS comparator and a full adder. ADCs and their subcomponents are important since along with general-purpose arithmetic-logic unit and microprocessor circuits, they enable a wide array of capabilities in HT electronics.

Prototyping, Low Volume Manufacturing and PDK

CoolCAD presently can fabricate four-inch (100mm) wafers in house for high temperature CMOS. CoolCAD also has an Alpha-version of a PDK, including a design rule checker and a layout versus schematic tool and SPICE models for our devices. Customers can work with us to design, layout and fabricate both digital and analog ASICs for operation above 300 ºC. Typical die size is 3mm by 3mm. Larger and smaller die are possible as well.

Addressing Challenges:

Here we briefly cover some challenges and our solutions.

Oxide Quality: It is a great advantage that SiC can grow a native oxide (SiO_2), but this material system has its own challenges, e.g. oxygen vacancies and carbon-related defects that can cause difficulties with interface and fixed-oxide charges, reducing reliability. We address these with physics-based modeling, combining Density-Functional Theory (DFT) and chemical reaction rate simulations, and experimental

work. We fabricate and test devices with various oxide growth/anneal methods (in O_2 or N_2O, with NO; oxidizing deposited Si; oxidation followed by oxide deposition) and gate stacks (high-k dielectrics; n- or p-poly, Al, or Ni gates), and have identified the preferred methods and materials for reliable high-temperature operation.

NMOS/PMOS Symmetry: For CMOS digital circuit design, balanced threshold voltages between NMOS and PMOS devices are needed. To this end we consider substrate type and doping, channel doping, and gate material choice. We also have to consider process-created tradeoffs in reliability or device characteristics; *e.g.*, a post-oxidation anneal improving NMOS performance may be detrimental to PMOS devices.

Scaling: Faster and lower-power device operation requires shorter gate lengths, which is the factor that has driven the silicon development roadmap over the last several decades. SiC processing is still relatively new, and has largely focused on power devices with other design concerns. We have recently gained access to a maskless projection lithography system which will allow us to achieve a standardized gate length in the vicinity of one micron and minimal capacitive overlap for increased speed of operation.

Summary:

We have developed a vertically-integrated SiC CMOS technology to enable general-purpose electronics applications at high temperatures above 400ºC, thereby expanding Moore's Law to very high-temperature applications.

[1] N. Goldsman, A. Akturk, Z. Dilli, M. A. Gross, U. Khalid, C. Darmody, "STRUCTURE FOR SILICON CARBIDE INTEGRATED POWER MOSFETS ON A SINGLE SUBSTRATE," Patent No. 11798938, 2023.

[2] N. Goldsman, A. Akturk, Z. Dilli, M. A. Gross, A. Abate, "Fabrication of High Temperature Silicon Carbide Transistor Device," U.S. Patent No. 11823899, 2023