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**Space-Proofing Power:
CoolCAD's Mission to
Radiation-Harden Power
Semiconductor Devices**



Illustration of Martian Base Camp

Abstract

In this paper, Dr. Akin Akturk delves into the critical issue of radiation-induced failures of power semiconductor devices utilized in space applications. He begins the discussion with an overview of NASA's technology roadmap objectives for power and energy storage in space, underscoring areas requiring advancement. Both terrestrial and space radiation hazards are then examined, with an emphasis on modes of failure and current strategies for mitigation. Dr. Akturk further delves into technical challenges and promising outcomes revealed from testing that are influencing the direction of engineering efforts to harden semiconductor power devices against radiation. He concludes by discussing CoolCAD Electronics' innovative silicon carbide (SiC)-based semiconductor design and fabrication approach that promises to deliver advanced radiation-hardened devices that will enable NASA's ambitious technology roadmap objectives.

NASA's Technology Roadmap for Space Power and Energy Storage

Boosting power and energy availability is a top priority in NASA's technology roadmap. Power is vital for achieving space mission objectives and is particularly crucial for NASA's future ambitions. Whether supporting astronauts on extended voyages to Mars or empowering propulsion of unmanned vehicles for scientific exploration of distant planets and asteroids, technological advancements are imperative for the realization of NASA's ambitious goals.

In my role at CoolCAD, I work with a pioneering team of engineers and scientists to develop the next-generation of silicon carbide (SiC)-based semiconductor power devices, engineered to operate reliably under the most demanding conditions. As one of a few chosen companies, we have been commissioned to play a pivotal role in advancing power and energy storage technologies so that NASA can meet its ambitious technology roadmap objectives. Technology goals include the development of:

- Next-generation radiation-hardened semiconductor power devices that are resistant to damage or malfunction caused by solar and galactic cosmic radiation (GCR) exposure, including low- and high-energy particles (neutrons, protons, electrons, and heavy ions) and x-rays and gamma-rays.
- Advanced power systems that are substantially more compact than current systems, achieving significant volume and mass reductions for future space missions. Currently these systems constitute approximately one-third of a spacecraft's mass at launch.

- Discrete power semiconductor devices for space applications that operate reliably at higher bias voltages and frequencies compared to existing systems. Presently, these devices undergo derating for space applications due to radiation effects, limiting their reliable operating voltage to less than 200 volts (V). To compensate, multiple derated devices are connected in series or parallel. This workaround not only complicates circuit design but also increases the volume and mass of the system.
- Power systems capable of withstanding tremendous forces of acceleration and deceleration - equivalent to 100 times the force of gravity. Additionally, these systems must endure extreme temperature variations, ranging from -270°C to 400°C .



Illustration of the International Space Station

The Silent Threat of Space Radiation

In the vast expanse of space there exists a silent yet potent threat: radiation. This invisible force can catastrophically damage sensitive electronics onboard spacecraft. As humanity's exploration of the cosmos advances, the need to understand and mitigate radiation hazards is critical to the success and safety of future space missions.

In the terrestrial environment, the Earth's atmosphere provides shielding against space radiation. Nevertheless, cosmic showers consisting of cosmic rays and solar particles manage to penetrate the atmosphere, interacting with nitrogen and oxygen atoms to generate secondary neutron particles ($E > 10 \text{ MeV/nucleon}$). These secondary terrestrial neutrons pose notable risks to electronics in commercial and military aircraft as well as ground vehicles.

In Low Earth Orbit (LEO), spanning from approximately 200 km to 1600 km above the Earth's surface, electronic devices are exposed to moderate

levels of space radiation, predominantly from protons and some heavy ion particles ($10 \text{ MeV/nucleon} < E < 500 \text{ MeV/nucleon}$). These particles pose a significant threat to electronics used in communication, navigation and imaging satellites, as well as other sophisticated spacecraft such as the International Space Station (ISS).

Above Low Earth Orbit (LEO) lie the inner and outer Van Allen radiation belts, comprised of three-dimensional donut-shaped clouds of high-energy protons and electrons. Here, billions of high-energy ionized particles originating from solar winds, are captured and held in place by the Earth's magnetosphere. The Van Allen belts are renowned for posing significant radiation threats to space missions. Astronauts in upcoming missions to the Moon will need to traverse through a portion of these belts and must do so quickly to limit radiation exposure. Additionally, sensitive electronics on spacecraft traveling through the Van Allen belts must be protected to safeguard against potential radiation damage.

Another notable radiation hazard is the South Atlantic Anomaly, located over the South Atlantic Ocean where the inner Van Allen radiation belt extends unusually close to Earth. Satellite and spacecraft orbiting several hundred kilometers above the Earth's surface are periodically subjected to intense ionizing radiation from this anomaly. Traversing through the South Atlantic Anomaly is thought to have contributed to the failures of the Globalstar network's satellites in 2007.

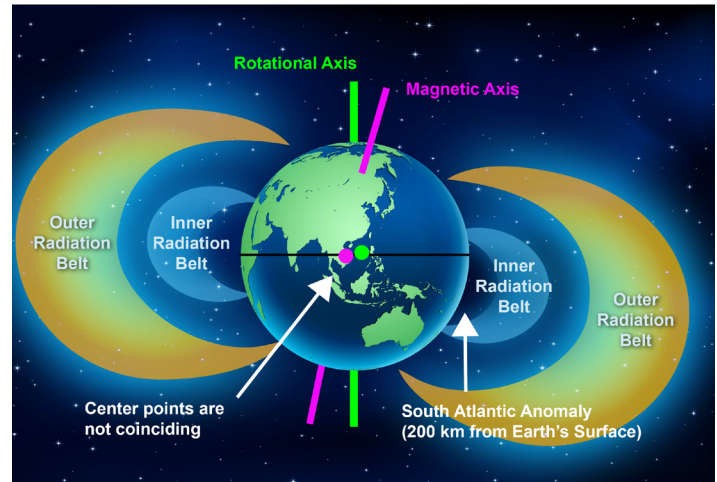
Beyond the Van Allen belts, radiation consists of a broad spectrum of cosmic and solar radiation, including x-rays, gamma-rays, protons, electrons and charged nuclei of elements ranging from hydrogen (alpha-particles) and helium (beta-particles) to the heavier elements, up to and including iron. Heavy ions, characterized by a charge and mass exceeding that of the helium-4 nucleus, are particularly hazardous due to their heightened charge and high energy levels ($E > 500 \text{ MeV/nucleon}$).

Battling Electronic Failures in the Cosmic Arena

The complex mixture of ionizing radiation in both the space and terrestrial environments can damage power semiconductor components in a variety of ways. From displacement damage to single event effects, damage can occur abruptly from a single ion strike or can develop gradually over time. Additionally, radiation damage can lead to either a transient malfunction or a catastrophic failure. Some of the most concerning modes of radiation-induced failure and common mitigation strategies are outlined below.

Displacement Damage (DD) is a non-ionizing failure mode. It occurs when particles with high kinetic energy collide with atoms within the crystal lattice of semiconductors, causing them to displace from their original positions. In the process of displacement, the atom leaves its position in the crystal structure, becomes interstitial and creates a vacancy. These displaced atoms, known as primary knock-ons, can trigger a cascade of additional atomic displacements. Over time, this phenomenon can significantly affect material properties and the electrical performance of devices. While shielding is commonly used to mitigate displacement damage, it comes with the drawback of added cost, volume and mass.

Total Ionizing Dose (TID) refers to a cumulative ionizing effect that results in a gradual failure. In Metal-Oxide-Field-Effect Transistors (MOSFETs),



absorbed radiation can create electron-hole pairs in the oxide layer (SiO_2) and within the bulk of the material. Within the bulk, electron-hole pairs quickly recombine or remove. Within the oxide, the electrons move toward the positively charged gate and are removed quickly. On the other hand, the holes (positively charged defects) hop at a slower pace toward the silicon (Si) interface due to a phenomenon called polaron hopping. As holes near the Si/SiO_2 interface, they become trapped and accumulate over time giving rise to a negative voltage shift. Additionally, as time goes on, some of these holes may give rise to additional interface trap defects due to bond breakage, resulting in a partial positive voltage shift.

In N-type MOSFETs, the buildup of positively charged holes near the Si/SiO_2 interface causes the device to leak current, much like a leaky faucet. In thick oxide MOSFETs, the result is a gradual decrease in threshold voltage (V_{th}), the gate voltage above which the device turns ON, until eventually the device remains ON even when a gate bias is applied to turn it OFF according to its specifications. In thin oxide MOSFETs, the decrease in threshold voltage remains relatively small; however, the MOSFET exhibits increased leakage along its device channel sidewalls.

In P-type MOSFETs, the accumulation of positively charged holes impedes the ability to turn the device ON, analogous to a corroded water valve. In thick oxide MOSFETs, this causes a gradual increase in the magnitude of V_{th} , the gate voltage below which the device turns ON. Over time, switching the device ON becomes increasingly difficult, until ultimately it ceases to function.

Shielding offers some protection from TID effects. However, the choice of shielding material is crucial.

For instance, aluminum effectively shields power devices from electrons and low-energy protons but proves ineffective against high-energy protons ($E > 30\text{MeV/nucleon}$). While there are a variety of materials that can be used for shielding, they all come with the drawback of added cost, volume and mass.

Device derating is another prevalent strategy used to address TID effects. Devices operating at higher bias voltages are likely to have thicker oxides, making them more susceptible to TID damage. This susceptibility is attributed to higher insulator volume which increases the accumulations of trapped hole defects.

Single Event Latch-Up (SEL) is a type of short circuit. It occurs when an ion strike triggers the activation of parasitic current through a portion of the circuit, increasing operating current beyond device specifications. The parasitic current persists as long as the device remains forward biased, requiring a power reset to clear the anomaly. Catastrophic SEL incidents can occur in less than a second, resulting in rapid failure. Predicting SEL occurrences is challenging since they are highly dependent on design parameters and manufacturing process variables. Mitigation strategies include redundancy and the implementation of a companion circuit for detection and device reset.

Single Event Burnout (SEB) and Single Event Gate Rupture (SEGR) are two different failure mechanisms which can be difficult to distinguish from one another. They are both the result of radiation-induced high current states in the device which occur suddenly and can result in catastrophic failure.

In Single Event Burnout (SEB), the high current state becomes self-sustaining due to electron tunneling assisted avalanche multiplication mechanisms, creating localized self-heating. Over time, high current can spread through the device. If localized self-heating is substantial it can lead to melting, cracking, and burnout along the ion track.

In Single Event Gate Rupture (SEGR), a single heavy ion strike can damage a MOSFET's oxide (SiO_2) dielectric layer, resulting in the formation of a conduction path. Under the influence of a critical transient gate field, leakage current increases, leading to catastrophic failure of the device.

The susceptibility to both SEB and SEGR is highly dependent upon bias voltage. Therefore, mitigation is achieved by derating devices for space missions. For example, a 100 V MOSFET may need to be derated down to 40 V due to these effects.

As mentioned above, MOSFETs intended for space applications are commonly derated to limit bias voltage below 200 V. To achieve power systems with higher voltages, multiple derated devices are connected in series or parallel. Although this approach reduces the risk of damage, it complicates circuit design while increasing the cost, volume and mass of the system.

Powering Beyond Current Technology Limits

While power devices like MOSFETs and diodes with voltage ratings exceeding 1700 V are available for terrestrial high-voltage power applications, their space-grade counterparts are limited to 200 V or less after derating. Despite advancements, such as utilizing hermetic sealing and radiation-hardening by design and process control, voltage capabilities of silicon-based power devices remain limited to 200 V, hindering the development of compact and lightweight power systems necessary to fulfill NASA's technology roadmap objectives.

Voltage constraints inherent in the current technology create significant challenges in power system design and operation. To achieve higher voltage and power outputs, multiple low voltage (derated) devices must be stacked or connected in series or parallel. For instance, the electrical power system of the International Space Station (ISS), comprised of extensive solar arrays, batteries, voltage converters, and switchgear, has pushed the boundaries of current radiation-hardened power semiconductor technology, capping power availability at roughly 10 kW due to circuit complexities, and size and weight concerns.

To achieve substantial mass and volume reductions, high-voltage radiation-hardened power devices are needed. Such devices would eliminate component stacking, paving the way for next-generation power converters and power distribution systems for space applications. Discrete radiation-hardened devices with ratings of 300 V and beyond would unlock the potential for high-power electric propulsion systems, currently limited to around 5 kW. Moreover, they would enable the implementation of 300 V (and beyond) solar arrays, a significant improvement over the existing 120V option, potentially reducing mission payload weight by several tons, depending on the mission.

Unraveling the Mystery of Radiation Hardening

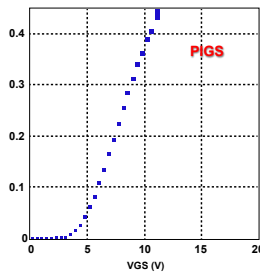
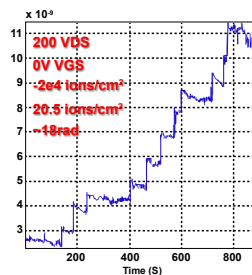
Engineers face a daunting task when working to fortify power devices against the hazards of space radiation. At CoolCAD, we began collaborating with NASA in 2017, propelling us on a journey of extensive research and testing, essential to understanding the complexities of the challenges before us. We have gained much insight through these investigative endeavors, uncovering previously unknown facts which have been instrumental in guiding the trajectory of our radiation-hardened products initiatives. Key findings include:

- Design parameters and semiconductor fabrication techniques play pivotal roles in susceptibility to radiation damage. These factors include circuit layout, P-N junction profiles, trench design, doping materials and levels, and the thickness of the passivating SiO₂ layer, among others. The diverse array of influential variables renders radiation-hardening by design and process a formidable challenge.
- A device's susceptibility to radiation damage can vary significantly between production lots, as well as among identical designs manufactured in different facilities with different equipment. These disparities in radiation performance highlight the importance of meticulous control over fabrication processes.
- Silicon (Si)-based semiconductor technology seems to be nearing its theoretical limits and struggles to provide discrete, very high-voltage, and radiation-resistant devices with favorable electrical characteristics such as low losses and high-frequency operation. In this context, alternative wide bandgap semiconductor materials such as GaN and SiC should be considered due to their favorable material characteristics.
- Commercially available silicon carbide (SiC)-based MOSFETs and diodes exhibit notable resilience to Total Ionizing Dose (TID) effects and Displacement Damage (DD) thanks to the inherent advantages conferred by their wide bandgap material properties. Furthermore, SiC devices boast superior thermal performance and switching speeds compared to traditional silicon-based counterparts.
- Commercially available silicon carbide (SiC)-based MOSFETs and diodes are susceptible to

Single Event Effects such as Single Event Burnout (SEB) and Single Event Gate Rupture (SEGR) when subjected to high-energy heavy ion strikes. Interestingly, the nature of this susceptibility varies depending on the gate and drain bias voltage applied during irradiation.

- At high drain bias voltage (greater than 33% of the device's breakdown voltage) a single high-energy heavy-ion strike in the active volume can cause irreparable catastrophic device failure. Meanwhile, at medium bias levels, increases in drain and gate currents are observed with device failures characterized by increased gate leakage during post-irradiation gate stress tests. However, at low voltage levels (as low as 10 to 20% of the rated voltage) a threshold is found, below which no measurable effects are observed following irradiation.

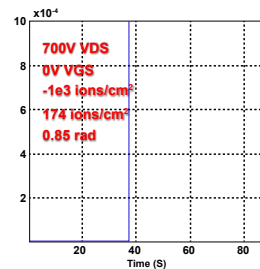
These findings suggest that a commercially available 1200 V SiC-based MOSFET would need to be derated to approximately 250 V to mitigate SEB events.



Drain current degradation at low voltage followed by failure during post irradiation gate stress test.



Test board used at Texas A&M University Cyclotron Facility



Failure with a single ion strike in active device area at high voltages.

*Heavy Ion Irradiation test setup and results for commercially available SiC power devices
Testing performed at Texas A&M University cyclotron facility*

- Gallium nitride (GaN)-based transistors (tested by JPL and Goddard researchers) demonstrate susceptibility to failure at approximately 50% of their rated voltage. Given that GaN devices are significantly overdesigned due to their lack of avalanche capability, this threshold is not significantly better than that of SiC. Moreover, GaN devices encounter additional challenges which are not present in semiconductor materials such as Si and SiC, including time-dependent

CoolCAD's Cosmic Crusade to Defy Radiation

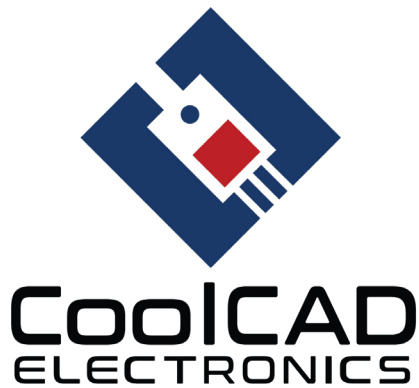
As experts in SiC-based semiconductor design and fabrication, CoolCAD Electronics has entered the forefront of innovation in the power semiconductor arena with a singular mission: to defy the relentless forces of radiation in space.

Building upon our vast experience in the semiconductor industry and our unparalleled proficiency in utilizing modeling and simulation tools for design optimization, we've dedicated ourselves to resolving the critical issues of SEB and SEGR failures in SiC-based power devices. Through meticulous modeling and simulation to define optimal design parameters and stringent control over fabrication processes, we've made substantial progress in overcoming these challenges.

We are proud to announce the successful demonstration of our prototype radiation-hardened SiC-based power switches, showcasing Single Event Burnout (SEB) threshold voltages reaching an impressive 900 to 1000 V under heavy ion exposure with Linear Energy Transfer (LET) exceeding 40 MeVcm²/mg and fluence of no less than 10⁵ ions/cm².

Our achievements thus far have us looking to the stars with renewed optimism. It has become increasingly evident that CoolCAD's mission extends far beyond merely overcoming the voltage limitations inherent in current technologies. We are pioneers, blazing a trail towards a new frontier of space exploration, empowering humanity to embark on journeys previously deemed impossible. We are proud to be part of NASA's extended team of innovators that are reshaping the boundaries of possibility to unlock the vast potential of cosmic discovery.





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About CoolCAD

CoolCAD Electronics is a leader in the development and fabrication of SiC-based power devices and high-temperature semiconductor electronics for aerospace, automotive, defense, geothermal development, green energy production, industrial furnace control, water purification, and oil and gas extraction. The CoolCAD team possesses a unique combination of expertise in electronics, semiconductor physics, fabrication, and design. They also excel at integrated and board-level circuit development and manufacturing. They have published 100s of research papers in professional scientific and engineering journals, and have multiple patents on their key discoveries in the area of wide bandgap SiC electronics.

To learn more about CoolCAD visit coolcadelectronics.com

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