# Radiation Tolerant Silicon Carbide High Voltage Transistors for Switching Power Converters

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Abstract-To achieve massive weight and volume savings in space and high-altitude missions, and to expand the operational range of critical applications, radiation-hardened high voltage and power devices are needed. These devices would pave the way for higher voltages and frequencies in power converters and power distribution systems. For example, use of higher voltages would give rise to mass savings in bus lines and solar array systems, and use of higher frequencies would yield mass and volume savings due to use of attendant compact passives such as capacitors and inductors. Therefore, to address the need for radiation-tolerant high voltage power components, we have been developing silicon carbide power MOSFETs that are less susceptible to single event effects, total ionizing dose drift and displacement damage. The single event burnout threshold voltage of these devices has been increased by more than 40% of that of commercial-off-the-shelf components. The total ionizing dose and displacement damage experiments also indicate a conservative radiation tolerance larger than 300 Krad (SiO<sub>2</sub>) and 10<sup>12</sup> p/cm<sup>2</sup>, respectively.

Keywords—radiation tolerant power, silicon carbide, burnout threshold, high voltage.

## I. INTRODUCTION

Current commercially-available SiC power devices, especially power MOSFETs and diodes, are very susceptible to heavy ion damage, rendering their use in space applications limited to a small voltage range that is not significantly better than the current silicon option.

Our goal is to design and fabricate silicon carbide power devices that are radiation tolerant. The novel SiC power switches are designed and built to operate in extreme environments. Here "extreme environment" specifically refers to high radiation exposure as well as relatively high temperature ambients. More specifically, the overarching goal is to provide the space industry with radiation-tolerant silicon carbide-based power switches tolerant to heavy ion LET of at least 40MeVcm<sup>2</sup>/mg and fluence of at least 10<sup>5</sup>ions/cm<sup>2</sup>. The target is to develop >900V (before derating) radiation-tolerant power devices.

Silicon (Si): Radiation-hardened silicon devices do exist; however, their power and voltage ratings are usually less than what are needed to achieve substantial improvements over Zeynep Dilli CoolCAD Electronics College Park, MD, USA zeynep.dilli@coolcadelectronics.com



**Fig. 1.** A heavy ion irradiation test board we previously used at Texas A&M University (TAMU) cyclotron facility. Drain and gate currents are continuously monitored approximately every 50ms during measurements. Commercially available SiC power devices suffer from terminal current degradations due to ion strikes at relatively low voltages. At high voltages, SiC power devices experience sudden failure events.

existing systems. Current systems are usually based on these silicon devices, and higher voltage and current platforms are achieved by stacking them up or connecting them in parallel, respectively. In addition to design complications stemming from use of multiple parts, this very granular design approach increases the number of parts used and the parasitic inductances and capacitance in the overall design, hence decreases the system reliability and efficiency.

Silicon Carbide (SiC): Earlier research on the characterization of radiation effects in silicon carbide power

devices reveal that silicon carbide power MOSFETs and diodes are very susceptible to damage from heavy ions (one of our earlier SiC power device heavy ion test boards is shown in Fig. 1 along with some example test data). In silicon carbide power MOSFETs, this attendant high LET heavy ion damage is found to change in character with bias during irradiation [1]. In the high bias range, which starts at approximately larger than one third of the breakdown or avalanche voltage, a single high LET heavy ion strike in the active volume is usually sufficient to irreparably damage the device. At medium biases, degradations or increases in drain and gate currents are observed, with or without equal degradation amounts mirroring at both of these terminals, but nonetheless correlating well. These degradations remain present even after the removal of the ion beam. For some devices that survive irradiation but exhibit some degradations in current during irradiation, device failures that are usually in the form of increased gate leakage are observed when performing post irradiation gate stress tests (see Fig. 1). At low biases that are as low as 10-20% of the rated voltage (~8-16% of the avalanche voltage), a threshold is found below which no measurable effects are observed after irradiation. This clearly dramatically limits the safe operating voltage of such silicon carbide power MOSFETs in most space environments. Moreover, similar degradation mechanisms are also observed in silicon carbide power diodes. As bias is increased beyond a threshold value, similar to the case with MOSFETs, degradations in terminal currents become apparent. This is followed by a catastrophic device failure at higher biases. Comparison between different types of vertical SiC power devices indicate a threshold field above which a catastrophic damage occurs irrespective of the device design. This indicates a damage mechanism that is purely a function of the electric field, and is possibly driven by electrical-thermal effects. At lower voltages, a drain or anode current degradation can also be related to a thermally-initiated process that is large enough to cause permanent damage but small enough to remain localized. In the case of MOSFETs, gate damage is also related to a temporary increase in oxide field, resulting in physical damages that might be explained by the percolation theory, latent ionizing and trapping induced electrical drifts, and subsequent increased gate leakage currents.

Gallium Nitride (GaN): Recent radiation testing of 600V and higher GaN transistors by Jet Propulsion Laboratory and NASA Goddard SFC researchers and others have shown failure susceptibility at about 50% of the rated voltage, or less. Considering that GaN devices are significantly overdesigned due to their lack of avalanche capability, this threshold is not significantly better than that of SiC. Additionally, even though GaN high electron mobility transistors (HEMTs) benefit from small active volume, and therefore relative protection from single event effects, these devices exhibit serious long-term reliability problems. For example, they suffer greatly from time dependent dielectric breakdown that is absent in nonpolar semiconductor materials such as Si and SiC. Also, growth of GaN on a nonnative substrate such as silicon results in a large number of different types of defects and defect concentrations, exposure of which to radiation for long periods of time may exacerbate the problem. Moreover, GaN vertical power device development is many years behind the SiC version development. A reason for this is a lack of high-quality



**Fig. 2.** a) An example resonant modular multi-level converter that can be used to triple the voltage using the same power devices on either side of the transformer. b) The realization of the same circuit using secondary side power devices that are rated for three times the voltage of the primary side switches.

substrates. Another reason is the great difficulty in activating dopant implants, especially of acceptor type. Lastly, the higher fields planned to be employed in GaN power devices, and the lower specific heat of gallium nitride, are likely to render thermal problems (such as those mentioned above for silicon carbide) worse, resulting in extreme challenges in the use of vertical GaN in a radiation environment without major amounts of derating.

Gallium Oxide  $(Ga_2O_3)$  and Diamond: Even though gallium oxide wafers can be grown with relative ease, their use in a power device in any significant way is yet many years behind.

A critical problem for this material is the absence of a p-type dopant. Even though there may be unique methods to achieve this type of doping, difficulties of these methods may overshadow for the relative ease of wafer production. Also, any bulk or vertical device made from this material is likely to have the same or worse thermal issues causing damage, such as those mentioned above. Lastly, growth, implantation, and processing are also huge problems facing devices fabricated using diamond.

### II. RADIATION HARDENED POWER CIRCUIT

The state-of-the-art technology for space-ready parts is <200V, which is significantly lower than the voltage rating of a ground-based equivalent component. This results in challenges in circuit design, and gives rise to less reliable and heavier systems. The state-of-the-art space power systems operate at 150V, significantly lower than higher voltages needed to achieve high SWAP (size, weight and power) in power conversion and delivery. An example state-of-the-art radiation tolerant silicon MOSFET is IRHMS57260SE, rated for 200V and has an on-resistance of 45m $\Omega$  at 29A. An example state-of-the-art radiation tolerant gate driver that can be used in conjunction with this power device is RIC7S113, which has a peak current of 2A.

To make higher voltage circuits, modular multi-level converters with devices stacked on top of each other and controlled in tandem are needed. Such converters greatly complicate circuit design, and they are prone to reliability issues due to parasitics and circuit induced transients.

An example for such a converter is a resonant modular multilevel converter, as shown in Fig. 2. Modular multi-level converters enable the use of radiation resistant low voltage silicon or gallium nitride power devices. The multi-level converter divides the rail-to-rail voltage evenly across multiple submodules, allowing bias stress sharing, and the usage of devices with lower voltage ratings. This helps alleviate the problem especially with single event effects (SEE) observed in devices with larger electric fields during operation, if devices with enough derating margins are employed. GaN high electron mobility transistors show resistance to radiation in the lower voltage range (<100V). At slightly higher voltages, a silicon device such as that described above can be used. However, a paradigm change is needed to achieve higher powers and reliability at the system level. This necessitates fabrication of radiation tolerant high voltage power devices such as those we develop and test.

#### III. RADIATION HARDENED HIGH VOLTAGE POWER DEVICES

*CoolCAD SiC Technology:* To address the need for power devices with higher voltage ratings that are needed for more reliable and high SWAP systems, we design and fabricate silicon carbide power devices that are radiation hardened. More specifically, we have developed techniques to improve the burnout threshold of silicon carbide power MOSFETs.

We have been developing a foundation for processing and fabrication of SiC power devices, integrated circuits, and related devices and circuits. Some of the processing steps developed to make silicon carbide devices are shown in Fig. 3a.



**Fig. 3.** a) Typical silicon carbide vertical power device fabrication steps. Silicon carbide processing methods have been developed in-house, and in conjunction with foundries to achieve high electrical performance at the device level. b) As a result of this background work and understanding of the internal operation of silicon carbide field effect transistors, advanced silicon carbide power devices with low specific on resistances have been fabricated. Typical performance characteristics of a 1200V 60m $\Omega$  device are plotted. c) Breakdown voltage wafermap of one of the CoolCAD's SiC 1200V 60m $\Omega$  power MOSFET is shown.

The critical steps in the fabrication of silicon carbide devices include implantation, dopant activation, oxidation, contact formation and interconnect / metal deposition. Typical electrical performance curves of one of our 1200V 60m $\Omega$  SiC power MOSFETs are included in Fig. 3b. We have found that the 1.2kV transistor yield for our production wafers, that have on-resistance of approximately 60m $\Omega$ , is greater than 95%. Breakdown voltage wafermap for a typical wafer is shown in Fig. 3c. In addition, the standard deviations for key performance parameters, listed in the datasheet, are typically within one percent of the median parameter value. The high yield and small standard deviation are indicative of high-quality epitaxial layers and fabrication processes.

Once standard process steps and designs were established, we started working on radiation hardening our silicon carbide power MOSFETs. The radiation experiments were performed at Brookhaven National Laboratory Tandem Van de Graaff facility. Fig. 4 shows the leakage plots for one of our SiC power MOSFETs during device development and testing. This experiment was pursued using the chlorine ion at this source. It has a SiC LET of approximately 18MeVcm<sup>2</sup>/mg. Here plot (a) shows the leakage versus run number, and plot (b) shows the runtime. Each run corresponds to a fluence of approximately 10<sup>5</sup>ions/cm<sup>2</sup>. For this device, there are eight runs in total with the bias changing from 300V to 1kV in 100V steps. The different colors show different runs; the dashed line represents the drainto-source leakage while the solid line represents the gate-tosource leakage. We see that there is not any significant leakage until halfway through run 5, during which the drain is biased at 700V. For the subsequent runs, the leakage continues to increase at greater rates until it rapidly hits compliance shortly after run 8 (bias is 1 kV) starts. Furthermore, we also recorded similar results when we use the calcium ion, which has a SiC LET of approximately 25MeVcm<sup>2</sup>/mg within the active device volume. This burnout threshold is significantly higher than those of devices that are commercially available.

The newly fabricated devices also exhibit favorable total ionizing dose response. They drift minimally with absorbed dose, as shown in Fig. 5. We performed total ionizing dose experiments using different DC bias conditions: VGS = 20VVDS = 0V, VGS = 0V VDS = 0V, and VGS = 0V, VDS = 0V, V1100V. At certain intervals, we interrupted the test and remeasured the devices to see how their thresholds had shifted, then they were placed back into the path of the radiation to again begin accumulating dose. Here we show the results for the maximum negative electric field on the gate (VGS = 0V, VDS = 1100V). In the positive case, the attendant threshold voltage shift was slightly higher. Here we see that after approximately 100kRad, the threshold has changed by about 0.4V. Additionally, after finishing dosing the MOSFETs, we allowed the devices to anneal at room temperature to determine if the threshold voltages would recover. The devices showed little to no meaningful recovery at room temperature.

In conclusion, the newly designed silicon carbide power MOSFETs exhibit burnout threshold in excess of 900V. They also show total ionizing dose tolerance above 100krad, rendering them suitable for use in various space applications.



**Fig. 4.** Leakage plots for one of our SiC power MOSFETs during irradiation using ions with LET of approximately 20MeVcm<sup>2</sup>/mg. (a) Leakage versus time. (b) Leakage versus run number. Drain (dashed) and gate (solid) experience burnout during the last run.



**Fig. 5.** (a) The curves show raw measurements, obtained using the diode-connected MOSFET configuration. Here, blue circles represent the pre-rad baseline; green, magenta, red, and black circles correspond to 5krad, 20krad, 90krad, and 117krad, respectively. Red stars indicate four days of room temperature anneal, and blue stars eleven days of room temperature anneal. We note that the general trend is a shift towards lower voltages. (b) The threshold voltage shifts with total ionizing dose. In this plot, the change in threshold voltage is with respect to the pre-radiation case. Each line color represents a different MOSFET measured during the test campaign. Variations in device characteristics, long cables and absorbed dose (due to slightly differing locations) give rise to small changes in response from device to device.

#### REFERENCES

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