

# Converting Power Electronics to SiC: Design Thermal and EMI Wins



Converting power electronic platforms from silicon (Si) or gallium nitride (GaN) to silicon carbide (SiC) has moved from theory to practice. Teams are doing it to gain higher efficiency, greater power density, and better thermal margins in traction inverters, fast chargers, industrial drives, photovoltaic inverters, and grid storage. SiC's wide bandgap, high critical field, and strong thermal conductivity enable higher blocking voltages, lower switching and conduction losses at elevated temperatures, and smaller magnetics at higher switching frequencies. Device costs are falling and 200 mm manufacturing is maturing. Today, the challenge is less about availability and more about executing the conversion well.

Every migration should start with a system audit. Set realistic efficiency targets, temperature limits, EMI requirements, and cost boundaries. Then choose the SiC device class and topology that fit your bus voltage and duty cycle. At 650 V, GaN often leads for ultra-compact, very high frequency supplies. SiC becomes attractive when designs need higher surge robustness, higher junction temperature, hard-switching capability, or strong short-circuit toughness. At 800 V and above, SiC is usually the default for traction, fast charging, and medium-voltage industrial gear thanks to voltage headroom, reliable body-diode behavior, and broad module availability.

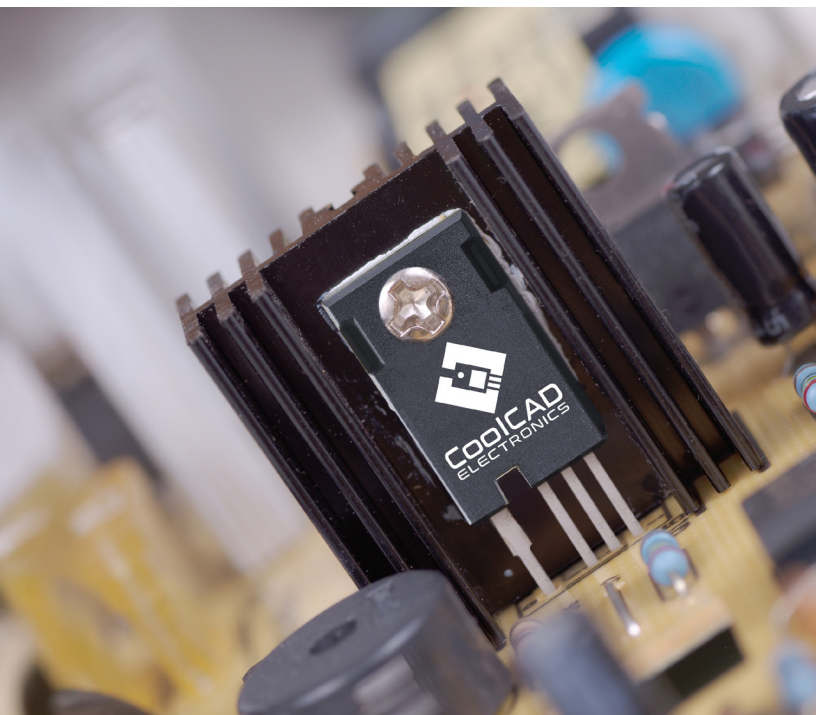
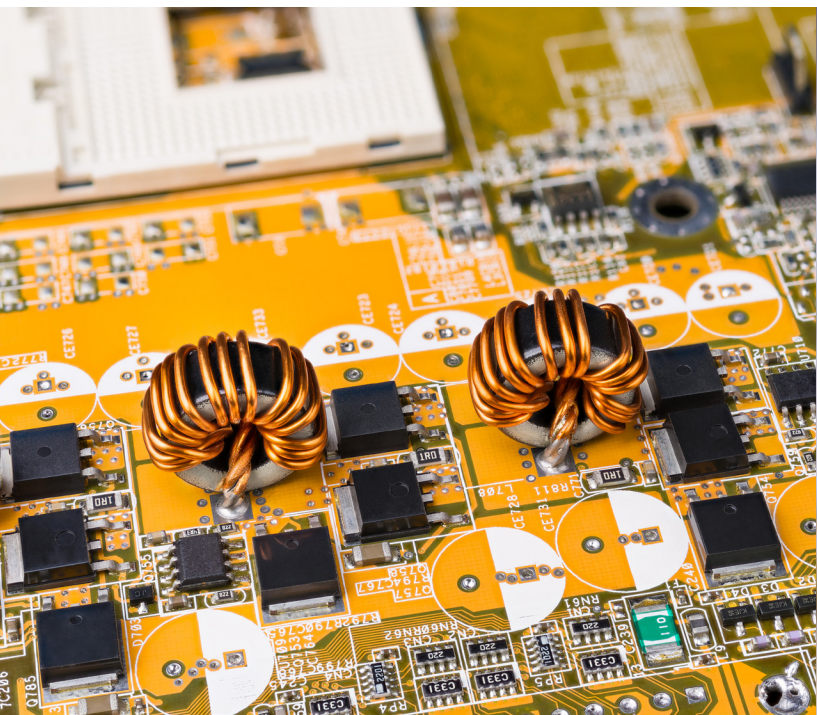


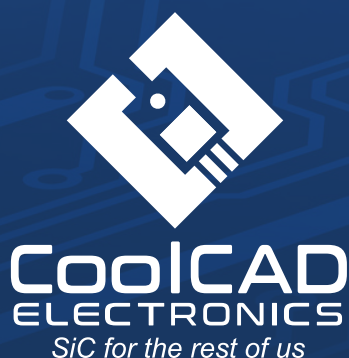
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Gate drive and switching dynamics change the most. SiC MOSFETs switch fast, with low output capacitance and an effective intrinsic diode. Rise and fall times can reach tens of  $\text{ns}$ . That cuts loss but increases  $\text{dv/dt}$  stress and common-mode noise. Use isolated drivers with high CMTI, Kelvin source returns, and tuned gate resistors. Add a Miller clamp or a small negative turn-off bias to prevent false turn-on at high  $\text{dv/dt}$ . Apply snubbers or RC damping only as needed so you do not give back the efficiency you gained. Because reverse-recovery is low, deadtime can be reduced. Prefer synchronous conduction, ZVS, or ZCS, and avoid long body-diode operation, which has a higher forward drop than the channel.

Thermal design is the next pillar. SiC can run hot, 175 to 200°C junction ratings are common, but only if heat leaves the die predictably. Many programs realize the full benefit by upgrading packaging: sintered die attach instead of solder, short interconnects, and packages with Kelvin source pins. Module designs gain the most from double-sided cooling and baseplates with AlN or AMB ceramics, which lower thermal resistance and support higher current density. After switching losses fall, right-size heatsinks and airflow. That often saves cost and volume, not just headroom.

Reliability and protection demand a mindset shift from IGBTs and, in some cases, from GaN. Short-circuit withstand time for SiC MOSFETs is only a few microseconds. Implement fast desaturation detection, soft turn-off, and tailored blanking in the driver. Avalanche and surge ratings are good, but they are not operating modes. Gate-oxide stability has improved with each generation, yet derate for your mission voltage and temperature. AEC-style qualification and stresses, HTGB, HTRB, power cycling, UIS, should mirror the real duty cycle, not a generic cookbook.





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Electromagnetics deserve early attention. Lower loss tempts higher switching frequency, but layout and parasitics set the ceiling. Revisit magnetics with lower-loss cores, interleaving, and minimized leakage to harvest both switching and conduction gains. Expect to retune common-mode filtering; fast edges increase displacement currents. Keep current loops compact, minimize gate-loop area, use low-inductance busbars, and add shielding where it buys margin. Good layout reduces filter burden and helps both conducted and radiated EMI compliance.

Three migration patterns dominate:

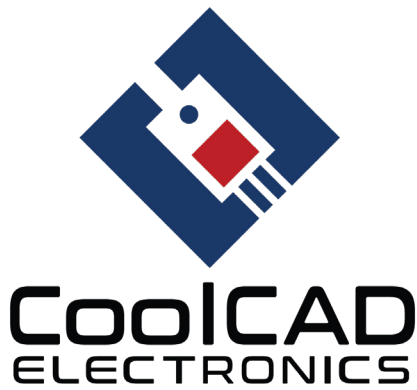
1. **Part-for-part replacement.** Swap Si or superjunction MOSFETs for SiC in hard-switched half bridges at equal or slightly higher frequency. This often yields 2 – 4 percentage points of efficiency gain and significant thermal relief with modest PCB changes.
2. **Topology shift.** Simplify the architecture using SiC's robustness. Examples include moving from a diode-bridge PFC plus DC-DC to a totem-pole PFC with a high-frequency transformer. Fewer parts, simpler control, and higher efficiency are common outcomes.
3. **Module-based redesign.** In traction or large industrial platforms, adopt modern SiC half-bridge or six-pack modules with low internal inductance and press-fit pins. This step delivers major gains in power density and dynamic performance.

The business case should be built at the system level. Per-die prices for SiC may still be higher than Si or some GaN parts, but system cost often falls. Efficiency gains allow smaller magnetics and reduced cooling hardware. Thermal headroom supports higher rated power in the same frame. Those offsets, plus improved field reliability, can more than cover the device premium.

Where GaN is the incumbent, SiC typically becomes the better choice when the platform moves to an 800 V bus, needs higher surge tolerance and short-circuit ruggedness, or must live in harsh thermal environments. Where Si IGBTs or superjunction MOSFETs are incumbents, SiC is compelling whenever efficiency, thermal relief, or power density unlocks a measurable BOM reduction or a performance step that the market values.

In short, converting from Si or GaN to SiC is an engineering optimization with known levers: disciplined gate-drive design, tight parasitic control, a modern thermal stack, and fast, well-tuned protection. Treat SiC as a platform, not a drop-in part. Designs that do this consistently achieve double-digit loss reductions, higher power density, and easier compliance with thermal and EMI limits. As devices and packaging improve, SiC conversions will keep resetting the baseline in high-voltage mobility, fast charging, renewable energy, and industrial power.





## CoolCAD Electronics LLC

7850 Walker Drive, Suite 140,  
Greenbelt, MD 20770

[contact@coolcadelectronics.com](mailto:contact@coolcadelectronics.com)

[coolcadelectronics.com](http://coolcadelectronics.com)



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