1.7kV SiC MOSFET (CC-17-40-744L) Unclamped Inductive Switching Test Report

Overview:

To evaluate the ruggedness of Silicon Carbide (SiC) power devices, the unclamped inductive switching test (UIS) is commonly used to determine the capability of a device to withstand avalanche events at a given peak current and avalanche energy for a certain number of pulses. This test is useful for characterizing the reliability of the device operating under inductive stress, which can occur during power converter switching and standard motor control operation. The specification corresponding to this test is typically listed as single pulse avalanche energy (EAS) or repetitive avalanche energy (EAR). For these tests, we chose to focus on measuring our device's EAR to provide a better metric for long-term reliability under inductive stress. The EAS can roughly be approximated as being 200× that of the EAR for similar current conditions (inductance must also be adjusted accordingly).

The objective of this report is to define a test setup for measuring the avalanche energy of CoolCAD's 1.7kV rated **CC-17-40-744L** device. This will help establish a safe operating area (SOA) for the power MOSFET under repetitive avalanche conditions. Additionally, the report outlines methods to safely operate the test setup while evaluating the device's repetitive avalanche ruggedness capability.

Due to the low prevalence of this specification for most commercial SiC power MOSFETs, there does not appear to be a standardized test that is used to determine the EAR. That is to say, although the circuit is standardized, the details of the test such as inductance, frequency, and number of cycles are not given in most of the datasheets containing this specification. As such, we have used several existing application notes as references for designing our own test procedure for characterizing the EAR for our devices. Most notably, Nexperia has published a very helpful article on the subject [1]. This article provides useful background information about the general test procedure, derivations on the avalanche energy calculations, and examples of safe operating area (SOA) graphs.

Additionally, Infineon appears to be the SiC device manufacturer that most consistently provides the avalanche energy specification in their datasheets, along with peak current, inductance, and supply voltage information [2]. Additionally, they have provided a useful guide for interpreting their datasheet information [3]. Using all these references, we were able to devise a repetitive avalanche energy test procedure for our devices.

[1] Nexperia, "Power MOSFET single-shot and repetitive avalanche ruggedness rating," Application Note AN10273, Rev. 6.0, Feb. 12, 2026. [Online]. Available: https://assets.nexperia.com/documents/application-note/AN10273.pdf

[2] Infineon Technologies AG, "IMZC140R038M2H 1400 V, 38 mΩ SiC MOSFET datasheet," [Online]. Available: https://www.infineon.com/assets/row/public/documents/60/49/infineon-imzc140r038m2h-datasheet-en.pdf

[3] Infineon Technologies AG, "Understanding and interpreting the CoolSiC™ MOSFET 1200 V datasheet," Application Note AN2025-10, Rev. 1.1, Mar. 2024. [Online]. Available: https://www.infineon.com/assets/row/public/documents/60/42/infineon-an2025-10-understanding-and-interpreting-the-coolsic-mosfet-1200v-datasheet-applicationnotes-en.pdf

Figure 1 illustrates the test circuit used to evaluate the avalanche ruggedness of a SiC MOSFET under an unclamped inductive switching event. Gate voltage pulses (Vgs) are applied to the device under test (DUT), causing the current through the inductor to ramp up until it reaches a peak value (Ipk) at a fixed input voltage (Vin). When the gate pulse ends, the DUT turns off. Because the inductor current cannot change instantaneously, it continues to flow, resulting in a voltage overshoot across the DUT. This voltage is then clamped at the device's avalanche breakdown voltage (VBR) until the inductor current decays to zero.

The following equation is used to determine the rate at which the avalanche current decays:

$$\frac{dIpk}{dt} = \frac{Vin - VBR}{L}$$

Since the breakdown voltage is always greater than the input voltage applied, the peak avalanche current starts decaying with a negative slope till it reaches zero. The avalanche energy dissipated is the area under power dissipated (PAV) waveform and is estimated from the following equation:

$$EAV = 0.5 \times \frac{VBR}{VBR - Vin} \times Ls \times Ipk^2$$

During tests, a 50V input is used, where the VBR is >2kV. Since (VBR - Vin) is comparable to VBR, the energy equation can be modified as follows:

$$EAV = 0.5 \times Ls \times Ipk^2$$

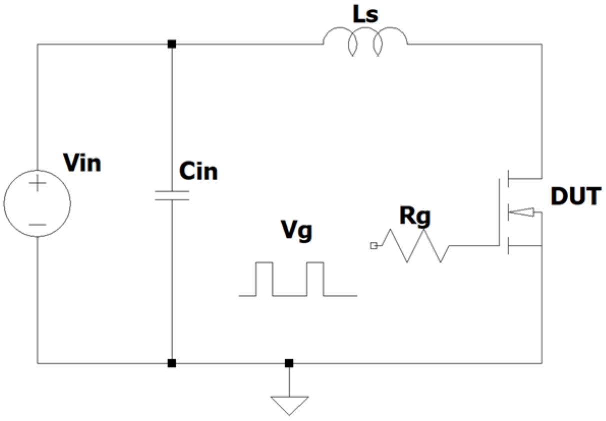

Figure 1: Unclamped inductive switching test circuit.

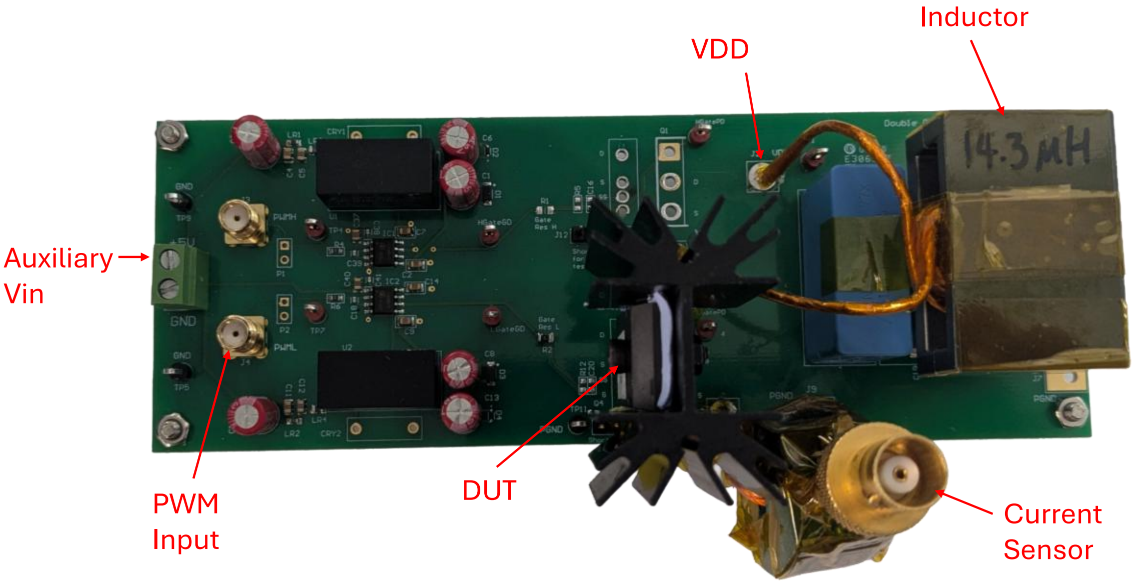

Figure 2: Unclamped inductive switching test setup.

The setup is based on our double pulses test circuit evaluation board: CC100A1KDPTV2
https://www.digikey.com/en/products/detail/electroverge/CC100A1KDPTV2/29180693?s=N4IgTCBcDaIMYHsEBs4EMAmIC6BfIA

Test Setup:

Figure 2 shows the physical test setup using a multipurpose custom designed printed circuit board. The device under test (DUT) is a **CC-17-40-744L** device that has undergone pretest sweeps to ensure the functionality of the device as well as provide a reference point. Once the UIS test is complete, these tests will be redone to see if there is any deviation from the pretest sweeps that may be indicative of device degradation. The DUT is connected to a heatsink to lower the case to ambient thermal resistance and ensure that this is not the limiting factor. A 50V DC voltage is given on the right side across the inductor and the DUT. The PWM signal is given from an external waveform generator, which is configured with a pulse width of 2.65us corresponding to a peak current of approximately 9A. These pulses are generated with a frequency of 50kHz, which we determined to be adequate time for the device to cool down between avalanche events while also not causing the test to run too long. Using this configuration, the device was pulsed continuous for 34 minutes, which corresponds to slightly over 100 million avalanche events, with no failure.

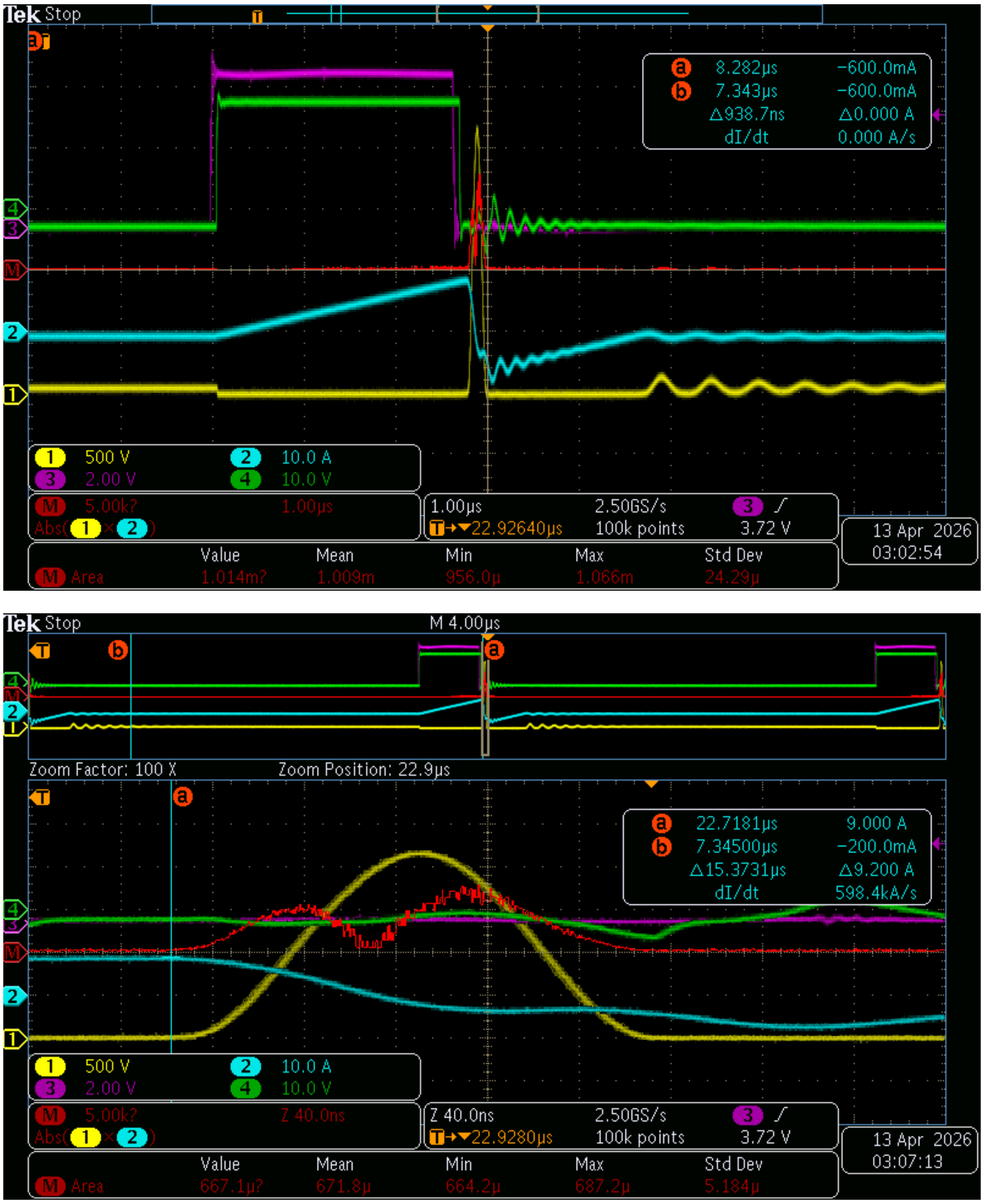

Figure 3: Waveforms for a single avalanche event: Top: Zoomed-out Bottom: Zoomed-in

Purple-Waveform generator Pulse; Green-DUT Vgs; Blue-DUT Ids; Yellow-DUT Vds; Red-DUT absolute power

Results:

Figure 3 shows some oscilloscope waveforms captured during the UIS test for a single avalanche event. A) shows a zoomed-out version and b) shows a zoomed-in version. Purple corresponds to the pulse from the external waveform generator, Green shows the pulse at the gate of the DUT, Blue shows the drain current of the DUT, Yellow shows the drain source voltage of the DUT, and red shows the absolute power dissipation of the device, which is calculated by the absolute value of the drain current multiplied by the drain source voltage. Additionally, the energy is measured as the integral of the absolute power. The value for the area of interest can be seen at the bottom of b), which is measured as **0.667mJ**. The corresponding power and temperature rise are approximately 33W and 12°C, respectively.

Once the avalanche test was concluded, the DUT's basic characteristics were retested to ensure there was no permanent damage to the device. **Figure 4** shows a comparison between the pre-test and post-test drain current versus drain voltage sweeps. Due to the insignificant difference between the two sweeps, we can conclude that the device was not damaged and did not degrade.

Lastly, using the avalanche test data, we created a peak current (I_{AL}) versus avalanche time (t_{AL}) safe operating area (SOA) curve. This is based on the fact that the value of $I_{AL}^2 \times t_{AL}$ is the parameter that determines the heating of the device during avalanching and exceeding the critical value leads to device overheating and subsequent failure. This critical value remains constant no matter the peak current, energy absorption, or avalanche time. **Figure 5** shows the SOA curve. Operating the device within the bounds of the blue curve should result in no permanent damage to the device.

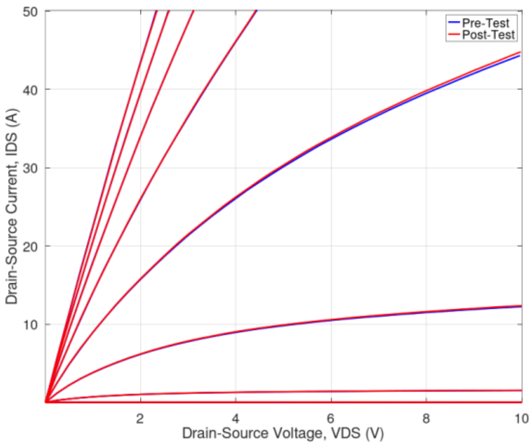

Figure 4: Pre-Test vs Post-Test drain current vs drain voltage sweeps for the DUT

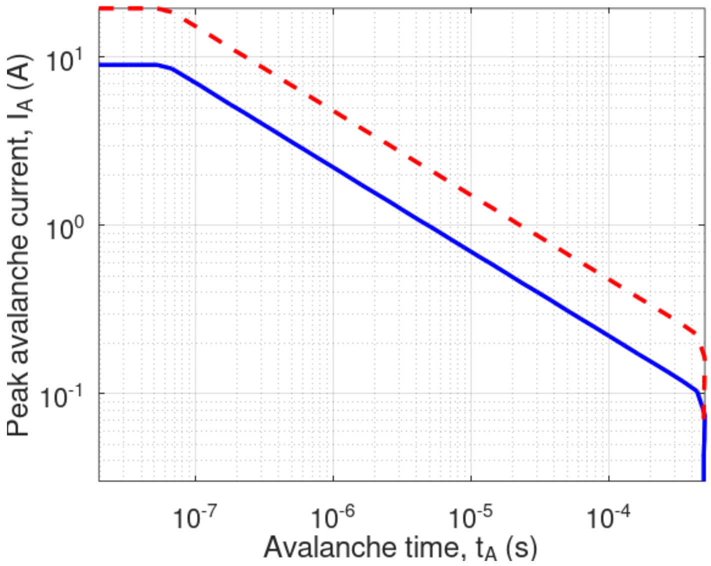

Figure 5: Peak avalanche current vs avalanche time safe operating area curve. Blue: Measured. Red: Calculated.

Summary and Comparison:

CC-17-40-744L:

EAR=0.667mJ (ID=9A, VDD=50V, L=14μH, Tambient= 25°C → ΔT≈12°C)

EARmax≈1.45mJ (for ΔT≈170°C and ID≈19A)

EAS≈290mJ (estimated)

Comparable SiC MOSFET

IMZC140R038M2H Datasheet: EAR=1.3mJ (ID=20.4 A, VDD = 50V, L = 6.2μH, Tambient= 25°C)

CAUTION: These devices and circuits are ESD sensitive. Use proper handling procedures.